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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

MI22-587

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Application Number

09/118,359

Filed

July 17, 1998

First Named Inventor

J. Dennis Keller

Art Unit

2823

Examiner

Michelle Estrada

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)☒ attorney or agent of record.
Registration number 46,791☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

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Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below".

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.09/118,359
 Filing Date July 17, 1998
 Inventor.....J. Dennis Keller
 Assignee.....Micron Technology, Inc.
 Group Art Unit.....2823
 Examiner Michelle Estrada
 Attorney's Docket No.MI22-587
 TitleMethods of Forming Floating Gate Transistors

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the rejection of claims 91-103. Claims 91-103 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Araki et al. (5,882,994) and Koido (2001/0014530). The basis for the rejection presented in the present action regarding claims 91-103 are identical to those in the immediately previous action dated January 26, 2005. Applicant's arguments and reasonings with respect to such rejection are fully set forth in the response filed April 25, 2005 at pages 8-13. Review and consideration of the content of such argument is respectfully requested.

It is noted with reference to MPEP § 2142 that the burden of establishing a prima facie case of obviousness is on the Examiner. According to MPEP § 2143 a prima facie case of obviousness requires a showing of some suggestion or motivation to combine referenced teachings; a reasonable expectation of success; and that the combined references must teach or suggest all of the claim limitations. A prima facie case regarding claims 91-103 has not been established for at least the reason that the cited references fail to teach or suggest all of the claim limitations.

As set forth in the response filed April 25, 2005, the combination of the cited references failed to teach or suggest “forming a first layer against and physically contacting the oxide-comprising layer, wherein the first layer comprises semiconductive material and a dopant, at least some of the dopant physically contacting the oxide-comprising layer,” as recited in claim 91. (see the April 25, 2005 response at pages 5-13).

As indicated at page 2 of the present action, Araki is relied upon as disclosing forming an oxide-comprising layer against and physically contacting a semiconductive substrate; forming a first layer over the oxide-comprising layer, wherein the first layer comprises a semiconductive material and a dopant; after forming the first layer, forming a second layer against and physically contacting the first layer, wherein the second layer comprises semiconductive material, the semiconductive material of the second layer having less dopant than the semiconductive material of the first layer, etc. (see page 2 of the present action). The Examiner at page 2 of the present action, acknowledges that “Araki et al do not disclose that the first layer comprising semiconductive material and a dopant physically contacting the oxide-comprising layer.”

The office action then goes on to state that Araki discloses various things about memory cells, phosphorus and polysilicon, how the structure can be used, how the structure of Araki avoids damage to the cell gate oxide film, and that it is possible to not only prevent damage to the cell gate oxide film due to the impurity in polysilicon, but it is also possible to control the bottom oxide film and minimize the natural oxide film formation. The Examiner then states that these teachings indicate that the disclosed formation of an undoped layer contacting the gate dielectric is merely desirable as opposed to necessary to produce a working device. The office action then goes on to state that the device would

not be inoperable and that the statements of Araki are to a preferred embodiment in that it would have been obvious to employ a doped semiconductive material in contact with the oxide-comprising layer with the expectation that Araki's disclosed advantages would not be obtained (page 3 of the present action).

Applicant believes that the Examiner is in error for at least the reason that a prima facie case of obviousness is not established by admitting a reference does not teach an element and then relying on same reference to meet the element by relying on an unidentified less desirable embodiment. As discussed above, a prima facie case requires that all elements of the claims be recited. The Examiner admits that Araki does not teach all elements of the present claims. The office action then goes on to state that the disclosed formation of an undoped layer contacting the gate dielectric is merely desirable as opposed to necessary to produce a working device without indicating where the claimed elements at issue are taught or suggested. This is an error for at least the reason that a reference cannot be relied on to teach an element of a claim as a less desirable embodiment on the one hand, and admittedly not teach the element on the other. The reference either teaches the element or it does not, and in this case, it does not.

As mentioned in the previous response, Araki describes two floating gate structures; the first floating gate structure being a prior art structure referenced in the background of Araki (Fig. 1, col. 1) and the second being Araki's floating gate structure (Figs. 4-8, col. 3 and 4). No other floating gate structures or embodiments of floating gate transistors are taught or suggested by Araki. Without additional teachings there are no other embodiments, less desirable or otherwise, taught or suggested by Araki. As such, the

Examiner's reliance on Araki to establish a prima facie case of obviousness in rejecting the pending claims is in error.

Independent claim 91 is believed to be allowable for at least the reasons discussed above and as more fully set forth in Applicant's April 25, 2005 response. Dependent claims 92-103 are allowable for at least the reason that they depend from allowable base claim 91.

Since the Examiner's maintained rejection of claims 91-103 are believed to be clearly erroneous and based upon improper reading of the applicant's remarks set forth in the response filed April 25, 2005, withdrawal of such maintained rejections is respectfully requested.

Respectfully submitted,

Dated: 10/26/05

By: 

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